

ABSTRACT

A self-clocking memory device comprises a memory array, a memory input circuit, and a memory control circuit. The memory input circuit is operable to receive an input clock signal and generate a memory operation initiation signal in response thereto, while the memory control circuit is operable to receive the memory operation initiation signal and generate one or more control signals to initiate a memory operation in response thereto. The memory control circuit is further operable to identify completion of the memory operation and generate a cycle ready strobe signal in response thereto. The memory input circuit receives the cycle ready strobe signal as an input and generates a next memory operation initiation signal in response thereto for initiation of a next memory operation.